**Control Unit Table**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Operation | Opcode | Reg  Dst | Write enb | ALU OP1 | ALU OP0 | ALU  src | sub | Store  enb | Load  enb | Ram to Reg | jump |
| Sub | 000 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Add | 001 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Addi | 010 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Beq | 011 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Sll | 100 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Sw | 101 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| jmp | 110 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| lw | 111 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |